Line", naming Pai-Hung Pan as inventor, and which is now U.S. Patent No. 5,739,066, the disclosure of which is incorporated by reference--.

In the Claims

Cancel claims 1-40 without prejudice.

Please add claims 41-52 as follows:

41. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising the steps of:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls and an interface with the gate dielectric layer;

forming sidewall spacers over the gate's sidewalls, the sidewall spacers joining with the gate dielectric layer; and

after forming the sidewall spacers, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith to oxidize at least a portion of the gate interface with the gate dielectric layer.

42. The method of claim 41, wherein the sidewall spacers comprise nitride.

43. The method of claim 41, wherein the gate comprises a first conductive layer a portion of which defines the interface, an overlying metal layer, and an electrically conductive reaction barrier layer interposed between the first layer and the overlying layer.

44. The method of claim 41, wherein the forming of the sidewall spacers includes:

depositing a first material over the gate;

depositing a second material over the first material;

anisotropically etching the first and second materials to a degree sufficient to leave the spacers over the gate's sidewalls, the spacers being defined by both the first and second material.

45. A semiconductor processing method of forming a conductive gate comprising:

forming sidewall spacers over a conductive gate's sidewalls sufficiently to cover all conductive material comprising said sidewalls; and

after forming the sidewall spacers, conducting an oxidizing step by channeling oxidants through a layer which underlies the gate and the sidewall spacers, and which is outwardly exposed laterally proximate the sidewall spacers.

46. The method of claim 45, wherein ~~said~~ the layer through which oxidants are channeled comprises a gate dielectric layer.

47. The method of claim 45, wherein the gate comprises polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal.

48. The method of claim 45, wherein the forming of the sidewall spacers comprises:

depositing a first material over the gate stack;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the sidewall spacers over the gate stack's ~~sidewalls~~.

49. The method of claim 45, wherein the forming of the sidewall spacers comprises:

depositing a first material over the gate stack;

anisotropically etching the first material to a degree sufficient to leave first sidewall spacers over the gate stack;

depositing a second material over the first sidewall spacers; and

anisotropically etching the second material to a degree sufficient to leave second sidewall spacers over the first sidewall spacers.

50. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising the steps of:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls disposed over the dielectric layer, the dielectric layer extending laterally outward of the sidewalls;

forming non-oxide material over the gate and dielectric layer;

anisotropically etching the non-oxide material to form non-oxide spacers over the sidewalls, the spacers joining with the gate dielectric layer; and

after anisotropically etching the non-oxide material to form the spacers, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate.

51. The method of claim 50, wherein the forming of the non-oxide material and the anisotropically etching thereof comprises:

depositing a first non-oxide material over the gate;

anisotropically etching the first non-oxide material to a degree sufficient to leave first spacers over the gate sidewalls;

depositing a second non-oxide material over the first spacers; and

anisotropically etching the second non-oxide material to a degree sufficient to leave second spacers over the first spacers.

52. A semiconductor processing method of forming a conductive gate comprising the steps of:

forming a patterned gate atop a substrate dielectric surface, at least a portion of the gate being conductive, the conductive portion comprising:

a polysilicon layer,

an overlying metal, and

a reaction barrier layer interposed between the polysilicon and the overlying metal;

covering a top and sidewalls of the gate with oxidation resistant material, said covering comprising:

depositing a first barrier material over the gate,

depositing a second barrier material over the first barrier material, and

anisotropically etching the first and second barrier materials to a degree sufficient to leave the oxidation barriers on the gate; and

exposing the substrate to oxidation conditions effective to oxidize at least a portion of the gate laterally adjacent the covered sidewalls adjacent the dielectric surface.